Form PTO-1390 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE (Rev. 11-2000)	Attorney's Docket Number 46309/271492
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371	U.S. Application No. (if known, see 37 CFR 1.5) 10/088424

International Application No.	International Filing Date	Priority Date Claimed
PCT/GB00/03528	13/09/2000 (13 September 2000)	13/09/1999 (13 September 1999)

Title of Invention

A LINEARISER FOR A SIGNAL HANDLING APPARATUS

Applicant(s) for DO/EO/US

KENINGTON, PETER; RING, STEVEN RICHARD; BENNETT, RICHARD MICHAEL

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a FIRST submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a SECOND or SUBSEQUENT submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This express request to begin national examination procedures (35 U.S.C. 371(f)). This submission must include items (5), (6), (9) and (21) indicated below.
4. ☐ The U.S. has been elected by the expiration of 19 months from the priority date (Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☐ is attached hereto (required only if not communicated by the International Bureau).
   b. ☒ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☐ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ An English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 20 below concern document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☒ A FIRST preliminary amendment.
14. ☐ A SECOND or SUBSEQUENT preliminary amendment.
15. ☐ A substitute specification.
16. ☐ A change of power of attorney and/or address letter.
17. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
18. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. ☐ Other items or information:

U.S. Application No. (if known, see 37 CFR 1.5)	International Application No.	Attorney's Docket Number
10/088424	PCT/GB00/03528	46309/271492

21. ☒ The following fees are submitted: CALCULATIONS PTO USE ONLY

BASIC NATIONAL FEE (37 CFR 1.492(a)(1)-(5)):

Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO.. $1000.00

International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO $890.00

International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO $710.00

International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) $690.00

International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) $100.00

ENTER APPROPRIATE BASIC FEE AMOUNT =				$ 890.00	
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).					
Claims	Number Filed	Number Extra	Rate		
Total claims	40 - 20 =	20	x 18.00	$ 360	
Independent Claims	6 - 3 =	3	x 84.00	$ 252	
Multiple Dependent Claims (if applicable)			+ 270.00	$	
TOTAL OF ABOVE CALCULATIONS =				$ 1,502	
☒ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.				$	
SUBTOTAL =				$ 751	
Processing fee of $130.00 for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f)).				$	
TOTAL NATIONAL FEE =				$ 751	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +					
TOTAL FEES ENCLOSED =				$ 751	
				Amount to be refunded:	$
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a. ☒ A check in the amount of $ 751 to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. 11-0855 in the amount of $ to cover the above fees. A duplicate copy of this sheet is enclosed.

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NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

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PATENTS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

PETER KENINGTON, ET AL.

Serial No. **TO BE ASSIGNED**

Filed: **CONCURRENTLY HEREWITH**
(National Phase of PCT/GB00/03528
filed September 13, 2000)

For: **A LINEARISER FOR A SIGNAL HANDLING APPARATUS**

Art Unit: To Be Assigned

Examiner: To Be Assigned

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, DC 20231

Sir:

Please enter the following amendments in the patent application identified above, before calculating the total amount of filing fee for that application.

In the Claims

Please cancel Claims 1-50, without prejudice.

Please add the following new claims:

51. A lineariser for reducing distortion of the output signal which signal handling equipment produces in response to an input signal, the lineariser comprising an extractor for extracting a portion of the input signal, a modifier for modifying the extracted signal to create non-linear components of reduced frequency therein, a generator for generating digitally a distortion signal from a delivered signal which is the modified signal and a combiner for combining the distortion signal with the input signal.

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Date: March 13, 2002

52. A lineariser according to Claim 51, wherein the modifier comprises a squarer for squaring the extracted signal.

53. A lineariser according to Claim 51, wherein the combiner comprises a mixer for mixing the distortion signal into the input signal.

54. A lineariser according to Claim 51, wherein the generator comprises a data store, wherein the data store is addressed by values of the delivered signal to responsively output corresponding values for the distortion signal.

55. A lineariser according to Claim 51, wherein the generator is arranged to generate a number of distortion components which are susceptible of independent control.

56. A lineariser according to Claim 55, wherein the generator comprises a splitter for splitting at least one distortion component into orthogonal components, each orthogonal component being susceptible of independent control.

57. A lineariser according to Claim 51, wherein the generator is arranged to combine a dc signal with the distortion signal.

58. A lineariser according to Claim 51, wherein the generator produces a number of components and further comprises an adjuster for removing lower order components appearing in at least one of the components.

59. A lineariser according to Claim 53, wherein the mixer comprises a splitter for splitting the input signal into orthogonal components.

60. A lineariser according to Claim 59, wherein the mixer mixes the distortion signal into one of the orthogonal input signal components.

61. A lineariser according to Claim 59, wherein the mixer mixes a dc component into one of the orthogonal input signal components.

62. A lineariser according to Claim 59, wherein the distortion signal comprises two orthogonal components and the mixer mixes each orthogonal signal component into a respective input signal component.

63. A lineariser according to Claim 61, further comprising a signal conditioner for conditioning the signal input to the generator so that the signal input maintains a substantially constant amplitude.

64. A lineariser according to Claim 51, further comprising a controller for adjusting a parameter of the distortion signal on the basis of feedback signal derived from the output signal.

65. A lineariser according to Claim 64, wherein the distortion signal comprises a number of components and the controller is capable of exerting independent control over at least one of them.

66. A lineariser according to Claim 64, wherein the controller generates at least one non-linear component of the signal input to the generator for correlation with the feedback signal to produce signals to control parameters of the distortion signal or components thereof.

67. A lineariser according to Claim 64, wherein the controller divides the signal input to the generator into components and correlates them with the feedback signal to produce signals to control parameters of the distortion signal or components thereof.

68. A lineariser according to Claim 64, wherein the controller divides the signal input to the generator into components and determines their amplitude in order to produce signals to control parameters of the distortion signal or components thereof.

69. A lineariser according to Claim 51, wherein the signal handling equipment comprises an amplifier.

70. A lineariser for reducing distortion of the output signal which signal handling equipment produces in response to an analogue RF input signal, the lineariser comprising an extractor for extracting a portion of the input signal, a generator for generating digitally a distortion signal from a delivered signal which is the extracted signal and a mixer for mixing the distortion signal into the input signal.

71. A lineariser according to Claim 70, wherein the generator comprises a data store, wherein the data store is addressed by values of the delivered signal to responsively output corresponding values for the distortion signal.

72. A lineariser according to Claim 70, wherein the generator is arranged to generate a number of distortion components which are susceptible of independent control

73. A lineariser according to Claim 72, wherein the generator comprises a splitter for splitting at least one distortion component into orthogonal components, each orthogonal component being susceptible of independent control.

74. A lineariser according to Claim 70, wherein the generator is arranged to combine a dc signal with the distortion signal.

75. A lineariser according to Claim 70, wherein the generator produces a number of components and further comprises an adjuster for removing lower order components appearing in at least one of the components.

76. A lineariser according to Claim 70, wherein the mixer comprises a splitter for splitting the input signal into orthogonal components.

77. A lineariser according to Claim 76, wherein the mixer mixes the distortion signal into one of the orthogonal input signal components.

78. A lineariser according to Claim 76, wherein the mixer mixes a dc component into one of the orthogonal input signal components.

79. A lineariser according to Claim 76, wherein the distortion signal comprises two orthogonal components and the mixer mixes each orthogonal signal component into a respective input signal component.

80. A lineariser according to Claim 76, further comprising a signal conditioner for conditioning the signal input to the generator so that the signal input maintains a substantially constant amplitude.

81. A lineariser according to Claim 76, further comprises a controller for adjusting a parameter of the distortion signal on the basis of a feedback signal derived from the output signal.

82. A lineariser according to Claim 81, wherein the distortion signal comprises a number of components and the controller is capable of exerting independent control over at least one of them.

83. A lineariser according to Claim 81, wherein the controller generates at least one non-linear component of the signal input to the generator for correlation with the feedback signal to produce signals to control parameters of the distortion signal or components thereof.

84. A lineariser according to Claim 81, wherein the controller divides the signal input to the generator into components and correlates them with the feedback signal to produce signals to control parameters of the distortion signal or components thereof.

85. A lineariser according to Claim 81, wherein the controller divides the signal input to the generator into components and determines their amplitude in order to produce signals to control parameters of the distortion signal or components thereof.

86. A lineariser according to Claim 70, wherein the signal handling equipment comprises an amplifier.

87. A lineariser for reducing distortion of the output signal which signal handling equipment produces in response to an analogue RF input signal, the lineariser comprising an extractor for extracting in portion of the input signal, a generator for generating digitally a distortion signal from a delivered signal which is the extracted

signal and a mixer for mixing the distortion signal into the input signal in a quadrature mixing process.

88. A lineariser for reducing distortion of the output signal which signal handling equipment produces in response to an input signal, the lineariser comprising an extractor for extracting a portion of the input signal, a modifier for modifying the extracted signal to create non-linear components of reduced frequency therein, a generator for generating digitally a distortion signal from a delivered signal which is the modified signal and a mixer for mixing the distortion signal into the input signal in a quadrature mixing process.

89. A method of reducing distortion of the output signal which signal handling equipment produces in response to an input signal, the method comprising extracting a portion of the input signal, modifying the extracted signal to create non-linear components of reduced frequency therein, generating digitally a distortion signal from a delivered signal which is the modified signal and combining the distortion signal with the input signal.

90. A method of reducing distortion of the output signal which signal handling equipment produces in response to an analogue RF input signal, the method comprising extracting a portion of the input signal, generating digitally a distortion signal

from a delivered signal which is the extracted signal and mixing the distortion signal into the input signal.

National Phase of PCT/GB00/03528
Preliminary Amendment

Version with Markings to Show Changes Made

Amendments in the Claims

In accordance with 37 C.F.R. 1.121(c) the following version of the claims as rewritten by the foregoing amendment shows all the changes made relative to the previous version of the claim.

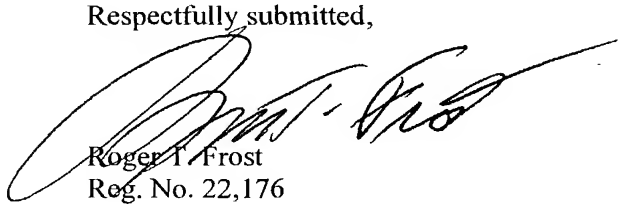
Claims 1-50 are cancelled and are replaced by new Claims 51-90.

REMARKS

New Claims 51-90 are substituted for the claims present during the international phase of this application. These new claims are drafted to exclude multiple dependencies; and to comply with 35 U.S.C. § 112, second paragraph.

The applicants request entry of these amendments and await examination in due course.

Respectfully submitted,



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(23890)

SIGNAL PROCESSING

This application relates to methods and apparatus for signal processing, in particular methods and apparatus for linearising, or reducing distortion appearing in, the output signal which a signal handling means produces in response to an input signal.

Predistortion schemes for reducing distortion appearing in the output of a non-linear amplifier are known. A synthesised distortion signal is added into the input to the amplifier. The distortion signal is arranged so that its addition tends to cancel any distortion imposed on the input signal by the amplifier during amplification.

According to a first aspect, the present invention provides a lineariser for reducing distortion of the output signal which a signal handling means produces in response to an input signal, the lineariser comprising means for extracting a portion of the input signal, means for modifying the extracted signal to create non-linear components of reduced frequency therein, means for generating digitally a distortion signal from the modified signal and means for combining the distortion signal with the input signal.

The invention may thus provide a flexible distortion reduction system which is capable of implementing relatively complex forms of distortion correction. The generation of reduced frequency components in the extracted portion of the input signal facilitates the use of digital signal processing in the generation and adaptation of the distortion signal for combination with the input signal to achieve the best possible distortion reduction therein. Since the lineariser according to the invention does not rely on local oscillator signals or any other form of reference from the host system of which it is a part, it can be implemented as a stand alone subsystem. This can be a significant benefit in many applications. It could even be located remotely from the rest of the system (e.g. a cellular radio base station).

According to a second aspect, the invention provides a lineariser for reducing distortion of the output signal which a signal handling means produces in response to an analogue RF

input signal, the lineariser comprising means for extracting a portion of the input signal, means for generating digitally a distortion signal from the extracted signal and means for mixing the distortion signal into the input signal.

The invention also provides a method of reducing distortion of the output signal which a signal handling means produces in response to an input signal, the method comprising extracting a portion of the input signal, modifying the extracted signal to create non-linear components of reduced frequency therein, generating digitally a distortion signal from the modified signal and combining the distortion signal with the input signal.

Furthermore, the invention also provides a method of reducing distortion of the output signal which a signal handling means produces in response to an analogue RF input signal, the method comprising extracting a portion of the input signal, generating digitally a distortion signal from the extracted signal and mixing the distortion signal into the input signal.

By way of example only, certain embodiments of the invention will now be described with reference to the accompanying figures, in which:

Figure 1 is a schematic diagram of a lineariser circuit;

Figure 2 is a schematic diagram of another lineariser circuit;

Figure 3 is a schematic diagram of a further lineariser circuit;

Figure 4 is a schematic diagram of a yet further lineariser circuit;

Figure 5 is a schematic diagram of another lineariser circuit;

Figure 6 is a schematic diagram of yet another lineariser circuit;

Figure 7 is a schematic diagram of a control scheme for a lineariser;

Figure 8 is a schematic diagram of another control scheme for a lineariser;

Figure 9 is a schematic diagram of a further control scheme for a lineariser;

Figure 10 is a schematic diagram of yet another lineariser circuit;

Figure 11 is a schematic diagram of yet another lineariser circuit; and

Figure 12 is a schematic diagram of yet another lineariser circuit.

As shown in Figure 1, a lineariser 100 is arranged to operate on the input to a radio frequency power amplifier (RF-PA) 110. The input signal to amplifier 110 is modified in a vector modulator 112 which precedes amplifier 110. The lineariser 100 produces in phase and quadrature predistortion components which are each mixed into a respective branch of the input signal within vector modulator 112. The input signal supplied to amplifier 110 is predistorted to counter distortion which the amplifier 110 causes to signals passing through it.

In general, the predistortion is derived from a portion of the input signal which is sampled using directional coupler 114 which precedes vector modulator 112. The operation of the square law detector will be discussed later. The sample taken from the input signal is manipulated using digital signal processor (DSP) 116. The DSP 116 provides three distortion components, each of which is split into orthogonal inphase and quadrature components by splitters 118,120,122. Each of the three inphase distortion components is then subjected to amplitude control by I channel controller 124. The adjusted inphase components are then summed to provide an inphase predistortion component which can be mixed into the input signal by vector modulator 112. Similarly, the three quadrature distortion components produced by splitters 118 to 122 are adjusted in amplitude under the control of Q channel controller 126, prior to being summed to produce the quadrature predistortion component for mixing into the amplifier input signal in vector modulator 112.

The controllers 124 and 126 monitor signals derived from feedback from the output of amplifier 110 (sampled at directional coupler 128) in order to determine the amplitude adjustments to be made to the various distortion components. The control process will be discussed in more detail later.

The lineariser 100 is a vector lineariser which mixes orthogonal predistortion components into respective orthogonal input signal components. A scalar lineariser having a more simple construction will now be described with reference to Figure 2. It will be apparent to a reader skilled in the art that the lineariser of Figure 2 can be extended to implement a vector linearisation scheme of a type shown in Figure 1.

Figure 2 illustrates a scalar lineariser 200 arranged to predistort the input signal to an RF power amplifier 210. The RF input signal intended for amplifier 210 is sampled by a directional coupler 212 to provide a signal from which the lineariser 200 can generate a predistortion signal for amplifier 210. The coupled port of directional coupler 212 feeds a splitter 214. One output of the splitter is used to down convert the frequency of the output of amplifier 210 for use in a controlled process, as will be described later. The other output of splitter 214 is supplied to a square law detector 216 which provides a baseband version of the sampled RF input. The square law detector 216 may be implemented by means of a mixer or multiplier with both of its inputs receiving the sampled RF input signal so as to multiply the input signal with itself. Alternatively, the square law detector may be implemented by means of a diode detector with an appropriate characteristic.

The output of the square law detector 216 is supplied to a digital signal processor (DSP) 218. The signal from square law detector 216 is converted to a digital signal by analogue to digital converter (ADC) 220. The digital signal from ADC 220 is provided to splitter 222. The splitter 222 provides the digital version of the output of square law detector 216 on three paths. The digital square law detector output is provided on path 224 as a second order distortion component. The digitised square law detector output is also supplied to squaring process 226 which provides a fourth order version of the input signal sampled from coupler 212. This fourth order signal is provided on path 228 as a fourth order

distortion component. The fourth order signal is also supplied to mixer 230 where it is mixed with the digitised square law detector output from splitter 222. The output of mixer 230 is supplied on path 232 as a sixth order distortion component. In high performance applications, it may be necessary to remove the unwanted second order component appearing in the sixth order distortion component signal. The second order distortion component can be simply subtracted directly from the sixth order distortion component since the second order distortion component has already been generated (by square order detector 216). The level of second order components in the sixth order signal is mathematically determined and hence perfect subtraction may be achieved without using an additional control scheme which could complicate the lineariser.

The fourth and sixth order distortion components are created by multiplying the digitised square law detector output with itself as required. It will be clear to the skilled person that this multiplicative process could be extended to the generation of eighth order distortion components and higher.

The second order distortion component on path 224 is adjusted in amplitude by variable gain element 234 under the control of controller 236. Similarly, amplitude adjustments are made to the fourth and sixth order distortion components on paths 228 and 232 respectively. The amplitude adjusted distortion components from paths 224,228 and 232 are summed at combiner 238 to produce a predistortion signal. The controller 236 adds a DC signal into the predistortion signal at combiner 240. The predistortion signal is then output from the DSP 218 via digital to analogue converter (DAC) 242 as an analogue predistortion signal.

In the main signal path, the RF power amplifier 210 is proceeded a vector modulator 244. The predistortion signal from DSP 218 is supplied to the Q channel mixer 246 of vector modulator 244. The DC signal introduced to the predistortion signal by controller 236 at combiner 240 allows mixer 246 to leak an appropriate amount of the RF input signal energy through the Q channel mixer. Similarly, the I channel mixer 248 is supplied with a DC signal from controller 236 to leak an appropriate amount of the inphase component of the RF input signal energy through that mixer. The mixers 246 and 248 operating on the

quadrature-split channels of the input signal allow the input signal vector to be steered through a full 360° and a range of amplitude levels. It is therefore possible to arrange the main input signal vector appropriately to match the predistortion signal vector which is only fed to the Q channel mixer as shown (alternatively, the predistortion signal could be supplied to the I channel mixer or to both the I and Q channel mixers).

The output signal of amplifier 210 is sampled by directional coupler 250 to provide a feedback signal for use by controller 236. The sampled output from coupler 250 and the sampled input signal from splitter 214 are mixed together in mixer 252 in order to frequency down convert the output signal sampled at coupler 250. This mixing process also has the effect of raising by 1 the order of each intermodulation distortion component present in the output of amplifier 210. The output of mixer 252 is supplied to controller 236 via ADC 254. The output signal sampled at directional coupler 250 will contain residual intermodulation distortion (IMD) products created by amplifier 210. In the output of mixer 252, each IMD product will be represented as a corresponding baseband signal at the next highest even order distortion frequency (e.g. a third order IMD product will produce a fourth order baseband signal in the mixer output after down conversion). These baseband even order IMD products may then be detected by the control scheme operated by controller 236 and used to adjust the relative amplitude levels of the distortion components on paths 224,228 and 232 which make up the predistortion signal. The detailed implementation of the control scheme operated by controller 236 will be discussed in more detail later.

Figure 3 illustrates a version of the linearisor of Figure 2 which has been modified to allow a low resolution analogue to digital converter 300 to be used to digitise the square law detector output. This is achieved by incorporating an automatic gain control loop in the linearisor to ensure that the input to ADC 300 remains broadly constant irrespective of the input signal level. A variable gain element 310 and an amplifier 312 operate in succession on the sampled input signal between coupler 314 and splitter 316. The DSP 318 monitors the amplitude of the output of square law detector 320 and produces a signal which controls the variable gain of variable gain element 310 such that the input to ADC 300 maintains a substantially constant amplitude. The DSP 318 can also measure the

power level of the signals received at ADC 300 and determine whether or not the lineariser needs to be active, i.e. if the power level of the input signals to the amplifier 322 undergoing linearisation is sufficiently low so that the amplifier 322 is operating within acceptable levels of distortion, then the lineariser can be deactivated.

The DC zone energy in the signal received at ADC 324 can be monitored to set the power output and/or gain of the amplifier 322 undergoing linearisation. This is achieved by adjusting, in equal proportion, the DC levels injected into the mixers of the vector modulator preceding amplifier 322.

In other respects, the lineariser of Figure 3 is similar in operation to the lineariser of Figure 2.

In the linearisers of Figures 2 and 3, a DC signal is added to the predistortion signal in the digital domain. Due to the dynamic range of this combined signal, a relatively high resolution and high speed DAC (242 in Figure 2) may be needed to perform the conversion to the analogue domain. The lineariser shown in Figure 4 is modified to ameliorate this potential disadvantage.

The lineariser 400 of Figure 4 operates in a similar manner to the lineariser of Figure 3. The lineariser 400 differs in that the addition of a DC signal to the predistortion signal occurs in the analogue domain at combiner 410. This permits the use of a relatively low resolution and low speed DAC 412 to convert the DC signal and a relatively low resolution and high speed DAC 414 for the distortion signal.

The lineariser 500 shown in Figure 5 is similar to that shown in Figure 4 except in that a multiplicative process is not used to generate the distortion components. As with the linearisers shown in Figures 2,3 and 4, the square law detector output signal is digitised and provided to splitter 510 within DSP 512. As previously, the splitter supplies a signal along a path 514 to provide the second order distortion component. The splitter 510 also provides an output to each of lookup tables 516 and 518. Lookup table (LUT) 516 contains values for the fourth order distortion component which correspond to particular

values of the square law detector output signal supplied by splitter 510. The LUT 516 is addressed by the current value of the signal from splitter 510 and retrieves the corresponding value for the fourth order signal, which is output on path 520 as the fourth order distortion signal.

If the LUT 516 does not contain a value for the fourth order distortion component corresponding to the current value of the signal from splitter 510, then an appropriate value for the fourth order distortion component can be interpolated. For example, the fourth order distortion component values stored in LUT 516 which correspond to the values of the square law detector output signal nearest to the true current value of the square law detector output signal can be used to determine a weighted average value for the fourth order distortion component value which should correspond to the current square law detector output signal value.

In a similar manner, the square law detector output signal is used to address LUT 518 which in response outputs corresponding values of the sixth order distortion component on path 522. Further LUT's could be provided and addressed by the square law detector output signal in order to produce additional distortion components. The distortion components are adjusted in amplitude and summed as described previously with reference to Figures 2,3 and 4.

In Figure 6, a baseband frequency, quadrature format input signal is provided and is quadrature upconverted using local oscillator 600 to produce a radio frequency input signal for non-linear power amplifier 610. A vector modulator arrangement is incorporated within the upconversion arrangement and comprises mixers 612 and 614 in the I and Q branches respectively of the upconversion process. As with the linearisers previously described, the predistortion signal is applied to mixer 614 and a DC signal is applied to mixer 612. However, in this embodiment, the baseband quadrature format input signal is applied directly to the DSP 616 in order to generate the predistortion signal. Subsequent to analogue to digital conversion, the baseband quadrature format input signals are combined and then squared at 618 to produce a second order distortion component on path 620 the squared output of process 618 is then squared again in process 622 to produce a

fourth order distortion component on path 624. The fourth order signal produced by squaring process 622 and the squared signal produced by squaring process 618 are multiplied together in mixer 626 to produce a sixth order distortion component. It will be appreciated that the multiplicative arrangement can be extended to the generation of eighth order and higher distortion components. The distortion components are then adjusted in amplitude and combined at 628 to produce the predistortion signal which is applied to mixer 614. It will be apparent that, in other respects, the lineariser of Figure 6 is similar in its operation to the foregoing embodiments.

Various control schemes for the amplitude adjustment of the distortion components will now be discussed.

Figure 7 shows a control scheme which may be used with, for example, the linearisers of Figures 2 to 5. Splitter 700 receives the digitised result of mixing the sampled input to the non-linear amplifier with its sampled output. This signal can be considered as the output of the amplifier down converted by its input. The signal supplied to splitter 700 thus contains fourth, sixth and eighth order components which correspond to the third, fifth and seventh order intermodulation distortion components created by the non-linear power amplifier undergoing linearisation. Splitter 700 supplies this signal to mixers 710,712 and 714. Splitter 716 receives the digitised square law detector output signal (which is a second order signal) and provides it to processes 718,720 and 722. Process 718 forms the square of its input and thus produces a fourth order output. Process 720 forms the cube of its input and thus produces a sixth order output. Process 722 forms the fourth order version of its input signal and thus produces an eighth order output signal. The outputs of processes 718,720 and 722 are each provided to the input of a respective one of mixers 710,712 and 714. Mixer 710 correlates the fourth order signal from process 718 with any residual fourth order intermodulation distortion present in the signal from splitter 700. The output of mixer 710 is supplied to an integrator which produces a control signal for the variable gain element in the second order distortion component path (i.e. in Figure 2, this would be variable gain element 234). It will be appreciated that, in effect, mixer 710 correlates the third order IMD distortion produced by the amplifier undergoing linearisation. Although the output of mixer 710 is used to control the gain of the second

order distortion component, it will be apparent that this second order distortion component gives rise to a third order distortion component when mixed into the input signal in the vector modulator. Similarly, the sixth order signal from process 770 is correlated with the sixth order IMD distortion in the signal from splitter 700 to produce a control signal for the variable gain element in the fourth order distortion component path. Likewise, the eighth order output of process 722 is correlated with the eighth order IMD distortion appearing in the signal from splitter 700 in order to produce a control signal for the variable gain element in the sixth order distortion component path within the lineariser. The results of the correlations performed by mixers 710,712 and 714 produce control signals that act individually to minimise the third, fifth and seventh order intermodulation distortion in the output of the power amplifier.

Figure 8 illustrates an alternative control mechanism wherein the result of mixing the non-linear amplifier output and input signals is subjected to fast Fourier transformation using process 800. The signal is thus transformed to the frequency domain and detectors 810,812 and 814 are each used to monitor the power present in a respective portion F1,F2 and F3 of the frequency spectrum. The control mechanism functions by detecting the amount of energy present at given frequency ranges and by minimising this energy on the assumption that it is dominated by the relevant order of intermodulation distortion.

A similar technique is illustrated in Figure 9, where the frequency separation is performed by using conventional bandpass filtering.

Figure 10 illustrates a vector lineariser which is in some respects similar to that described with reference to Figure 1. The lineariser of Figure 10 differs from that of Figure 1 in that the quadrature channels used separately to derive the inphase and quadrature predistortion components applied to the respective mixers of the vector modulator are created in the analogue domain using quadrature splitter 1000. Vector linearisers provide the advantage of being able to set the relative phase and amplitude of each of the distortion components in the predistortion signal independently allowing the lineariser to more accurately cancel the intermodulation distortion produced by the non-linear power amplifier.

A modification to the basic system described with reference to previous figures is shown in Figure 11. Here, the vector modulator has been replaced with an amplitude modulator, shown here as a mixer 1100, and a phase shifter 1110. The operation of the circuit is similar to that described previously, but in this case only two quadrants are available for control (on the assumption that the phase shifter has a range of 90°, which is typical for a single stage RF phase shifter). The two quadrants are obtained by supplying the predistortion signal to mixer 1100 in an inverted or non-inverted form.

As a further modification, the main signal path, prior to the amplifier 1112 undergoing linearisation, now employs a directional coupler 1114 configured with its minimum path loss in the main signal path. The low path loss of directional coupler 1114 and the low loss through the phase shifter 1110 helps to ensure that the overall system noise figure is kept to a minimum. The alternative approach of providing a vector modulator as described previously within the amplifier undergoing linearisation (i.e. after one or more low noise stages) is sometimes not possible due to the limited signal handling capability of such devices when good linearity performance is required.

The lineariser of Figure 11 also employs a second variable phase shifter 1116 in the input reference path which provides an input signal to output signal downconverting mixer 1118. Phase shift element 1116 is provided to ensure that the detected output signal level from mixer 1118 is maximised, irrespective of the phase shift through amplifier 1112. Phase shifter 1116 is varied by the DSP 1120 until a maximum signal level is detected (resulting in the two signals supplied to mixer 1118 being in phase). This setting can then be stored and the intermodulation distortion reduction control process initiated, with the maximum possible signal to noise ratio being available for the detection process. Without phase shift element 1116, it is possible that the two signal supplied to mixer 1118 could be in quadrature phase and hence the downconversion ADC 1122 would receive a null input signal. The controller 1124 might then assume that either the intermodulation distortion has been cancelled, and/or that the gain of the circuit is too low. In both of these case, the controller 1124 would then take either no action (when action is in fact required) or inappropriate action.

Clearly, there is a wide range of alternatives to the phase shift elements and amplitude modulation devices introduced in Figure 11. For example, time delay elements could be used in place of the phase shift elements 1110 and 1116 in Figure 11. A further alternative configuration of the various couplers and splitters in the main signal path is shown in Figure 12. Furthermore, the variable phase shift element used in Figures 11 and 12 in the input reference path to the downconverting mixer could equally well be inserted in the output sampling path instead, i.e. the phase shifting element could be located between output coupler 1200 and mixer 1210.

It will be apparent that the distortion generating process performed by the DSP in any of the previously described linearisers can be adapted to produce additional, higher order distortion components of the predistortion signal (e.g. eighth order or higher).

CLAIMS

1. A lineariser for reducing distortion of the output signal which a signal handling means produces in response to an input signal, the lineariser comprising means for extracting a portion of the input signal, means for modifying the extracted signal to create non-linear components of reduced frequency therein, means for generating digitally a distortion signal from a delivered signal which is the modified signal and means for combining the distortion signal with the input signal.

2. A lineariser according to claim 1, wherein the modifying means comprises means for squaring the extracted signal.

3. A lineariser according to claims 1 or 2, wherein the combining means comprises means for mixing the distortion signal into the input signal.

4. A lineariser for reducing distortion of the output signal which a signal handling means produces in response to an analogue RF input signal, the lineariser comprising means for extracting a portion of the input signal, means for generating digitally a distortion signal from a delivered signal which is the extracted signal and means for mixing the distortion signal into the input signal.

5. A lineariser according to any preceding claim, wherein the distortion generating means comprises storage means, wherein the storage means is addressed by values of the delivered signal to responsively output corresponding values for the distortion signal.

6. A lineariser according to any preceding claim, wherein the distortion generating means comprises means for generating a number of distortion components which are susceptible of independent control.

7. A lineariser according to claim 6, wherein the distortion generating means comprises means for splitting at least one distortion component into orthogonal components, each orthogonal component being susceptible of independent control.

8. A lineariser according to any preceding claim, wherein the distortion generating means comprises means for adding a dc signal into the distortion signal.

9. A lineariser according to any preceding claim, wherein the distortion generating means comprises means for multiplying the delivered signal with itself repeatedly.

10. A lineariser according to claim 9, wherein the distortion generating means produces a number of components and further comprises means for removing lower order components appearing in at least one of the components.

11. A lineariser according to any one of claims 3 to 10, wherein the mixing means comprises means for splitting the input signal into orthogonal components.

12. A lineariser according to claim 11, wherein the mixing means mixes the distortion signal into one of the orthogonal input signal components.

13. A lineariser according to claims 11 or 12, wherein the mixing means mixes a dc component into one of the orthogonal input signal components.

14. A lineariser according to claim 11, wherein the distortion signal comprises two orthogonal components and the mixing means mixes each orthogonal signal component into a respective input signal component.

15. A lineariser according to any preceding claim, further comprising means for conditioning the signal input to the distortion generating means so that it maintains a substantially constant amplitude.

16. A lineariser according to any preceding claim, further comprising means for monitoring the amplitude of the extracted signal and determining whether to place the lineariser in an operative condition.

17. A lineariser according to any preceding claim, further comprising control means for adjusting a parameter of the distortion signal.

18. A lineariser according to claim 17, wherein the control means uses a feedback signal derived from the output signal to determine the adjustments to the distortion signal.

19. A lineariser according to claim 17 or 18, wherein the distortion signal comprises a number of components and the control means is capable of exerting independent control over at least one of them.

20. A lineariser according to any of claims 17 to 19, wherein the parameter adjusted by the control means is amplitude.

21. A lineariser according to any one of claims 17 to 20, wherein the control means generates at least one non-linear component of the signal input to the distortion generating means for correlation with the feedback signal to produce signals to control parameters of the distortion signal or components thereof.

22. A lineariser according to any one of claims 17 to 20, wherein the control means divides the signal input to the distortion generating means into components and correlates them with the feedback signal to produce signals to control parameters of the distortion signal or components thereof.

23. A lineariser according to any one of claims 17 to 20, wherein the control means divides the signal input to the distortion generating means into components and determines their amplitude in order to produce signals to control parameters of the distortion signal or components thereof.

24. A lineariser according to any preceding claim, wherein the signal handling means is amplifying means.

25. A lineariser substantially as hereinbefore described with reference to any of Figures 1 to 10.

26. A method of reducing distortion of the output signal which a signal handling means produces in response to an input signal, the method comprising extracting a portion of the input signal, modifying the extracted signal to create non-linear components of reduced frequency therein, generating digitally a distortion signal from a delivered signal which is the modified signal and combining the distortion signal with the input signal.

27. A method according to claim 26 wherein the modifying step comprises squaring the extracted signal.

28. A method according to claim 26 or 27, wherein the combining step comprises mixing the distortion signal into the input signal.

29. A method of reducing distortion of the output signal which a signal handling means produces in response to an analogue RF input signal, the method comprising extracting a portion of the input signal, generating digitally a distortion signal from a delivered signal which is the extracted signal and mixing the distortion signal into the input signal.

30. A method according to any one of claims 26 to 29, wherein the distortion generating step comprises addressing a storage means by values of the delivered signal to responsively output corresponding values for the distortion signal.

31. A method according to any one of claims 26 to 30, wherein the distortion generating step comprises generating a number of distortion components which are susceptible of independent control.

32. A method according to claim 31, wherein the distortion generating step comprises splitting at least one distortion component into orthogonal components, each orthogonal component being susceptible of independent control.

33. A method according to any one of claims 26 to 32, wherein the distortion generating step comprises adding a dc signal into the distortion signal.

34. A method according to any one of claims 26 to 33, wherein the distortion generating step comprises multiplying the delivered signal with itself repeatedly.

35. A method according to claim 34, wherein the distortion generating step produces a number of components and further comprises removing lower order components appearing in at least one of the components.

36. A method according to any one of claims 28 to 35, wherein the mixing step comprises splitting the input signal into orthogonal components.

37. A method according to claim 36, wherein the mixing step comprises mixing the distortion signal into one of the orthogonal input signal components.

38. A method according to claim 36 or 37, wherein the mixing step comprises mixing a dc component into one of the orthogonal input signal components.

39. A method according to claim 36, wherein the distortion signal comprises two orthogonal components and the mixing step comprising mixing each orthogonal distortion signal component into a respective input signal component.

40. A method according to any one of claims 26 to 39, further comprising conditioning the signal used to generate the distortion signal in the distortion generating step so that it maintains a substantially constant amplitude.

41. A method according to any one of claims 26 to 40, further comprising monitoring the amplitude of the extracted signal and determining whether to subject the output signal to the distortion reduction method.

42. A method according to any one of claims 26 to 41, further comprising a control step of adjusting a parameter of the distortion signal.

43. A method according to claim 42 wherein the control step uses a feedback signal derived from the output signal to determine the adjustments to the distortion signal.

44. A method according to claim 42 or 43, wherein the distortion signal comprises a number of components and the control step comprises exerting independent control over at least one of them.

45. A method according to any one of claims 42 to 44, wherein the parameter adjusted by the control step is amplitude.

46. A method according to any of one of claims 42 to 45, wherein the control step comprises generating at least one non-linear component of the signal used to generate the distortion signal in the distortion generating step for correlation with the feedback signal to produce signals to control parameters of the distortion signal or components thereof.

47. A method according to any one of claims 42 to 45, wherein the control step divides the signal used to generate the distortion signal in the distortion generating step into components and correlates them with the feedback signal to produce signals to control parameters of the distortion signal or components thereof.

48. A method according to any one of claims 42 to 45, wherein the control step divides the signal used to generate the distortion signal in the distortion generating step into components and determines their amplitude in order to produce signal to control parameters of the distortion signal or components thereof.

49. A method according to claim 26 to 48, wherein the signal handling means is amplifying means.

50. A method substantially as hereinbefore described with reference to any one of Figures 1 to 10.

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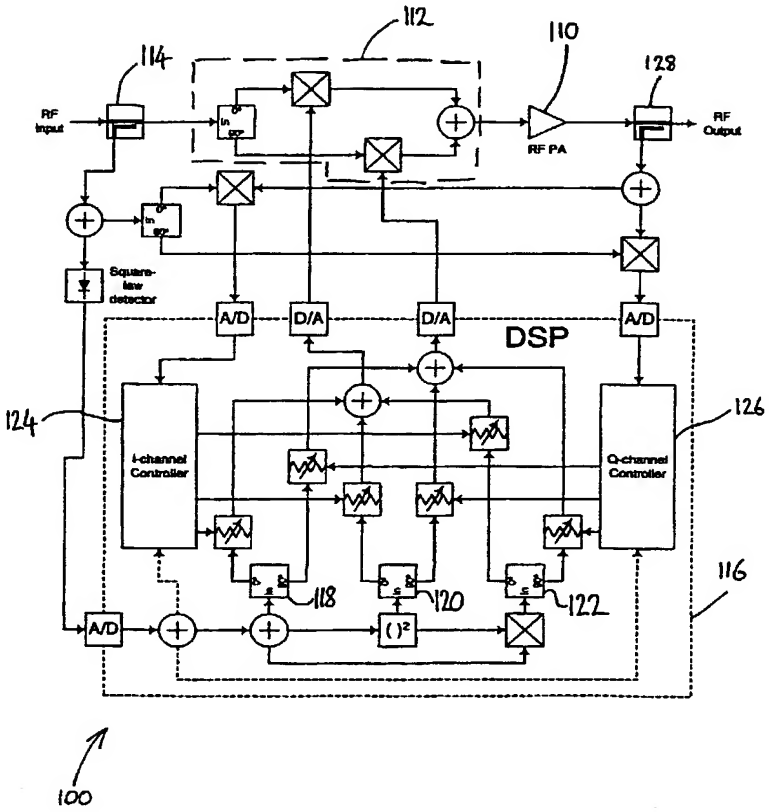
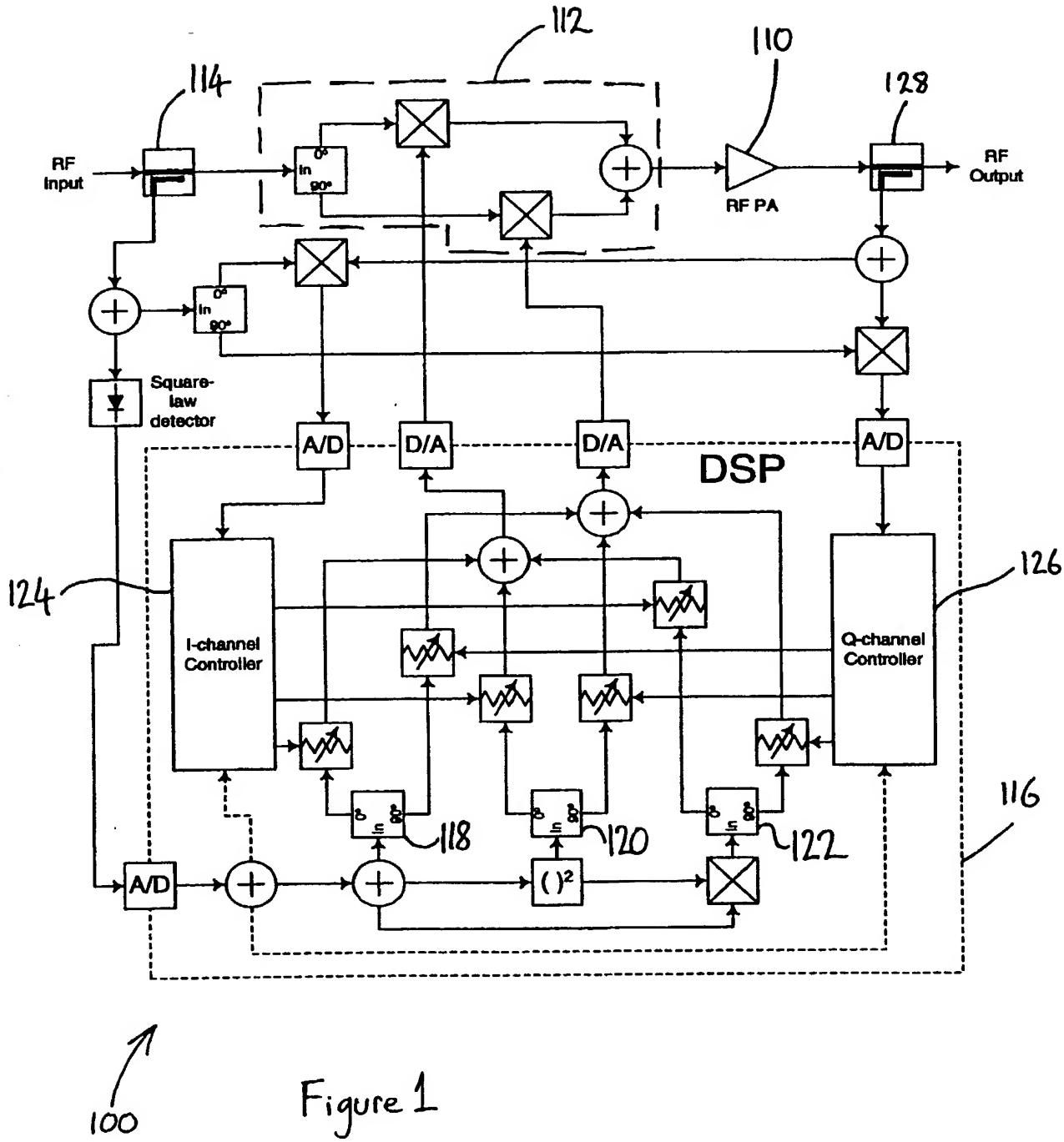
[Continued on next page]

(54) Title: A LINEARISER FOR A SIGNAL HANDLING APPARATUS



(57) Abstract: A lineariser (100) for reproducing distortion present in the output of an amplifier (110) (or other signal handling device) generates a predistortion signal from the amplifier input. The predistortion signal is mixed into the amplifier input signal using, for example, a vector modulator (112). The predistortion signal may be derived in a quadrature format, the orthogonal components of the predistortion signal being mixed into separate mixers of the vector modulator. The predistortion signal is generated by multiplying the input signal with itself repeatedly to generate components of distortion which are susceptible of independent control. The predistortion signal is generated digitally using DSP (116). A multiplier or mixer may be used to square the sampled input signal to produce a reduced frequency signal which the DSP can use to gennerate the predistortion signal. Another lineariser mixes the predistortion signal into the input signal during up conversion.

WO 01/20775 A1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114
128
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RF Output
RF PA
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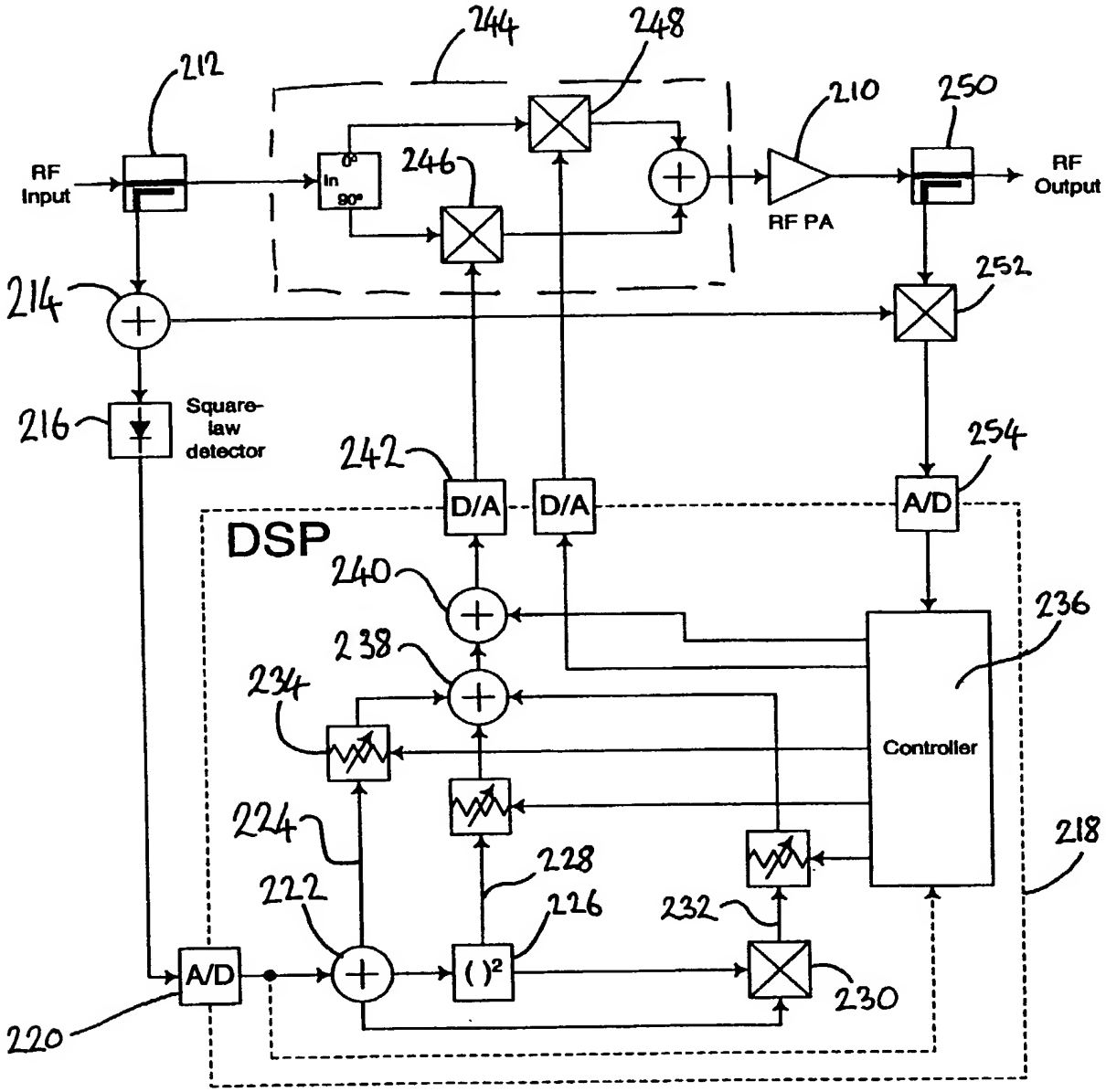
In
90°
Square-law detector
A/D
D/A
D/A
A/D
DSP
124
I-channel Controller
Q-channel Controller
126
116
118
120
122
A/D
( )²
100

Figure 1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212
210
250
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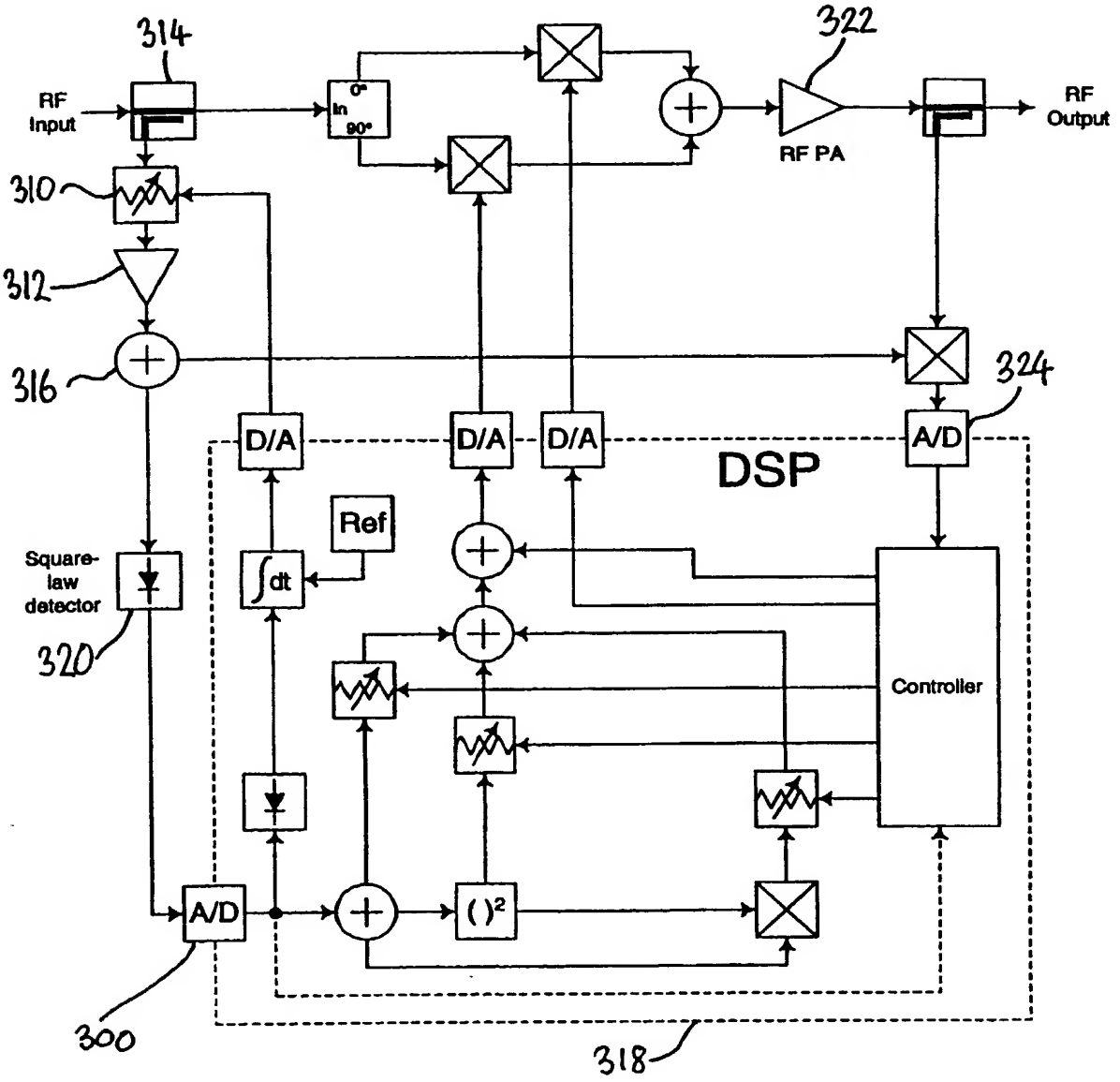
0°
In
90°
246
RF PA
RF Output
252
214
216
Square-law detector
242
D/A
D/A
A/D
254
DSP
240
238
236
234
Controller
224
218
228
222
226
232
A/D
( )²
230
220

200

Figure 2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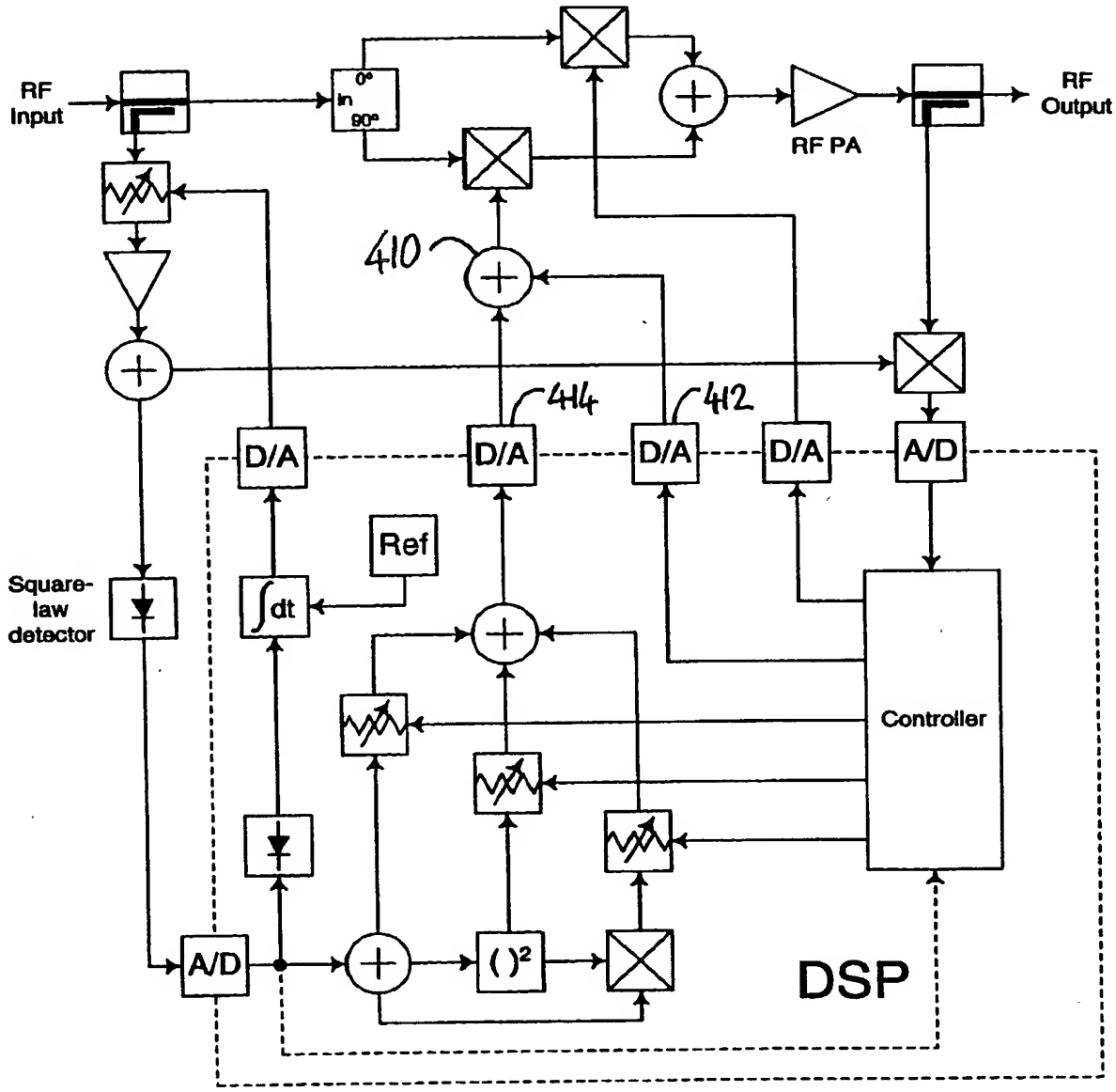
322
RF Input
0°
In
90°
RF PA
RF Output
310
312
316
324
D/A
D/A
D/A
A/D
DSP
Ref
∫dt
Square-law detector
320
Controller
A/D
( )²
300
318

Figure 3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In
90°
RF PA
RF Output
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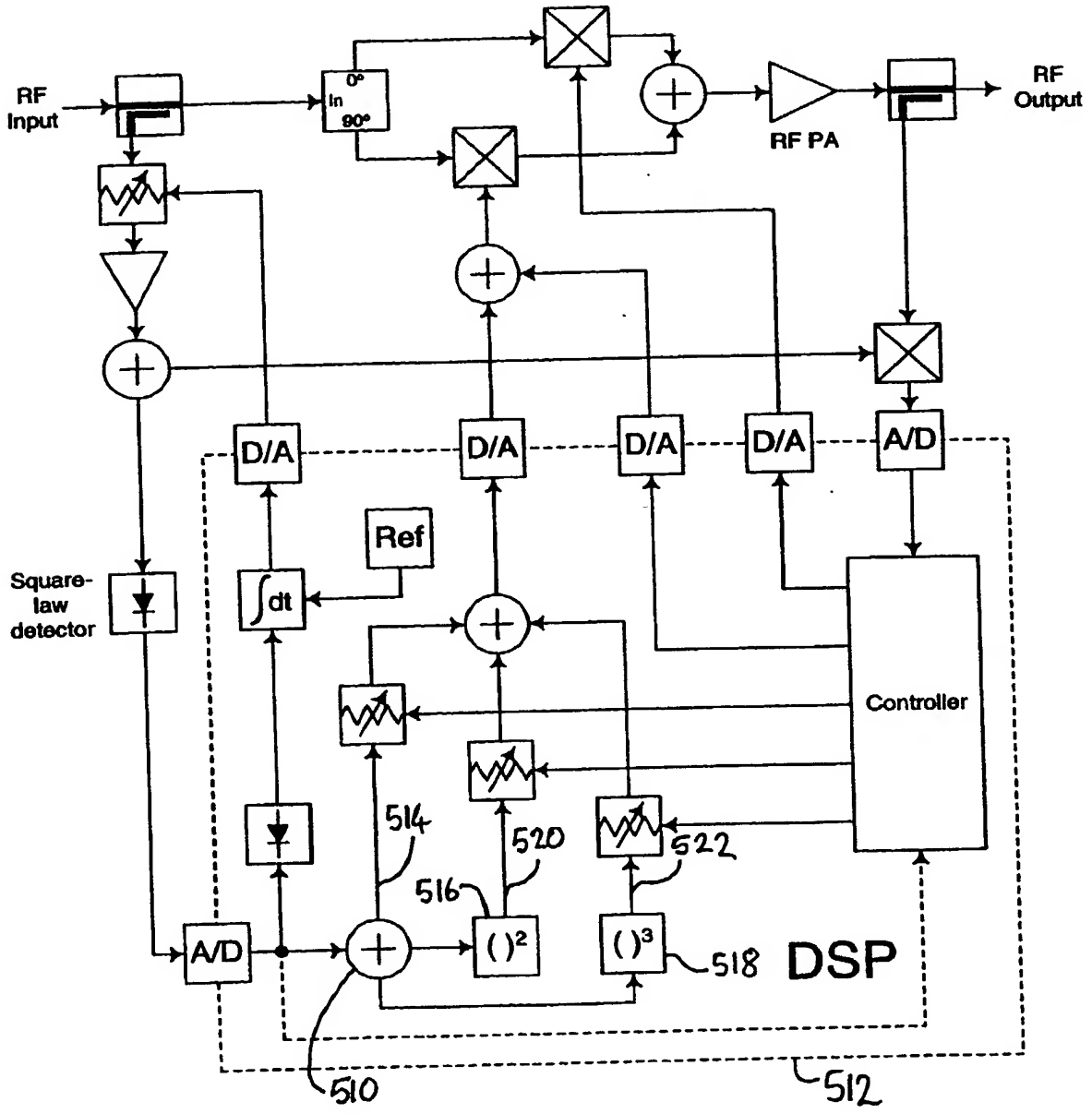
414
412
D/A
D/A
D/A
D/A
A/D
Ref
∫dt
Square-law detector
Controller
A/D
( )²
DSP
400

Figure 4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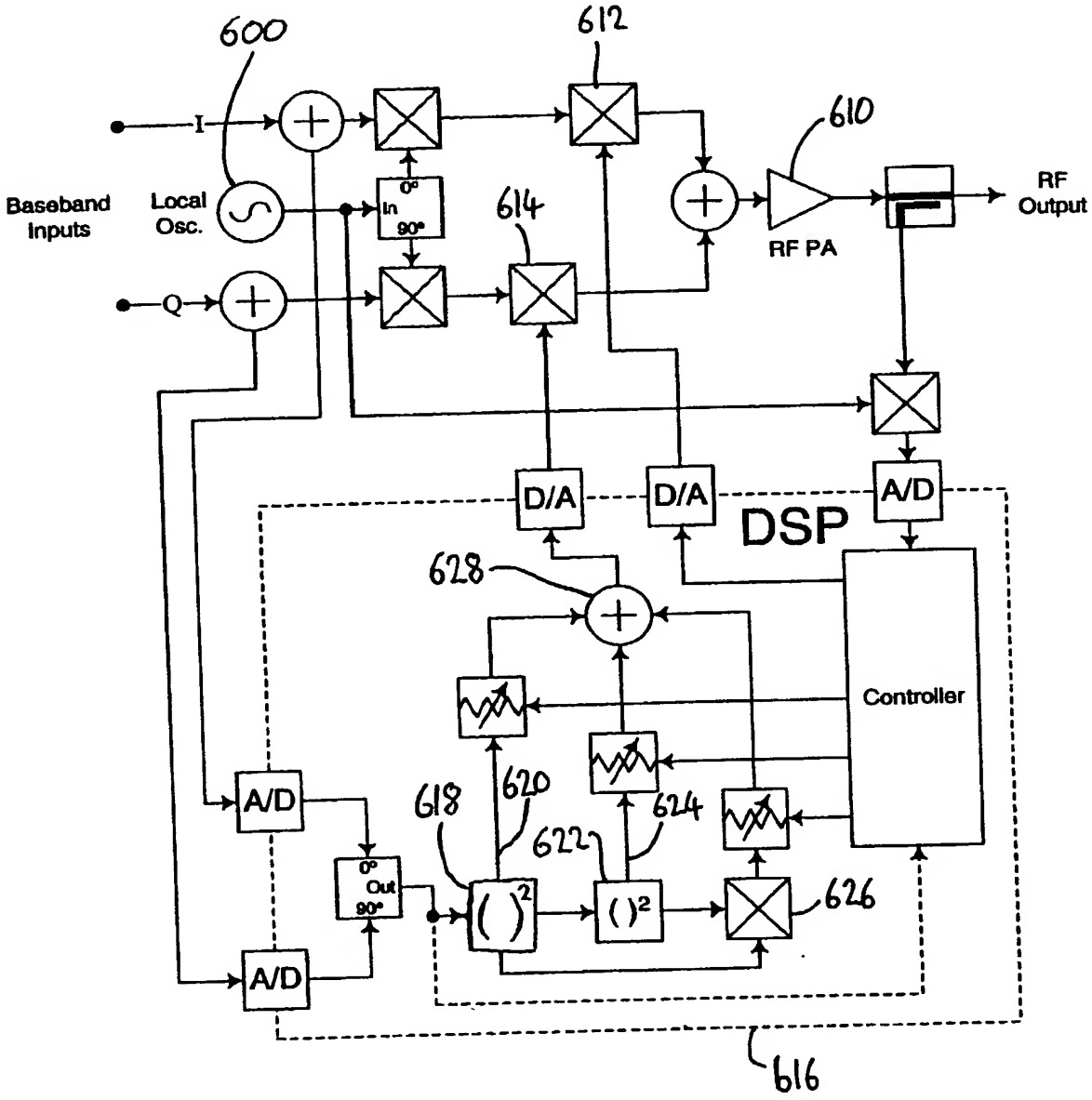
0°
In
90°
RF PA
RF Output
D/A
D/A
D/A
D/A
A/D
Ref
∫dt
Square-law detector
Controller
514
520
522
516
A/D
()²
()³
518
DSP
510
512
500

Figure 5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612
610
I
Baseband Inputs
Local Osc.
0° In 90°
614
RF PA
RF Output
Q
D/A
D/A
A/D
DSP
628
Controller
A/D
618
620
624
622
0° Out 90°
( )²
( )²
626
A/D
616

Figure 6

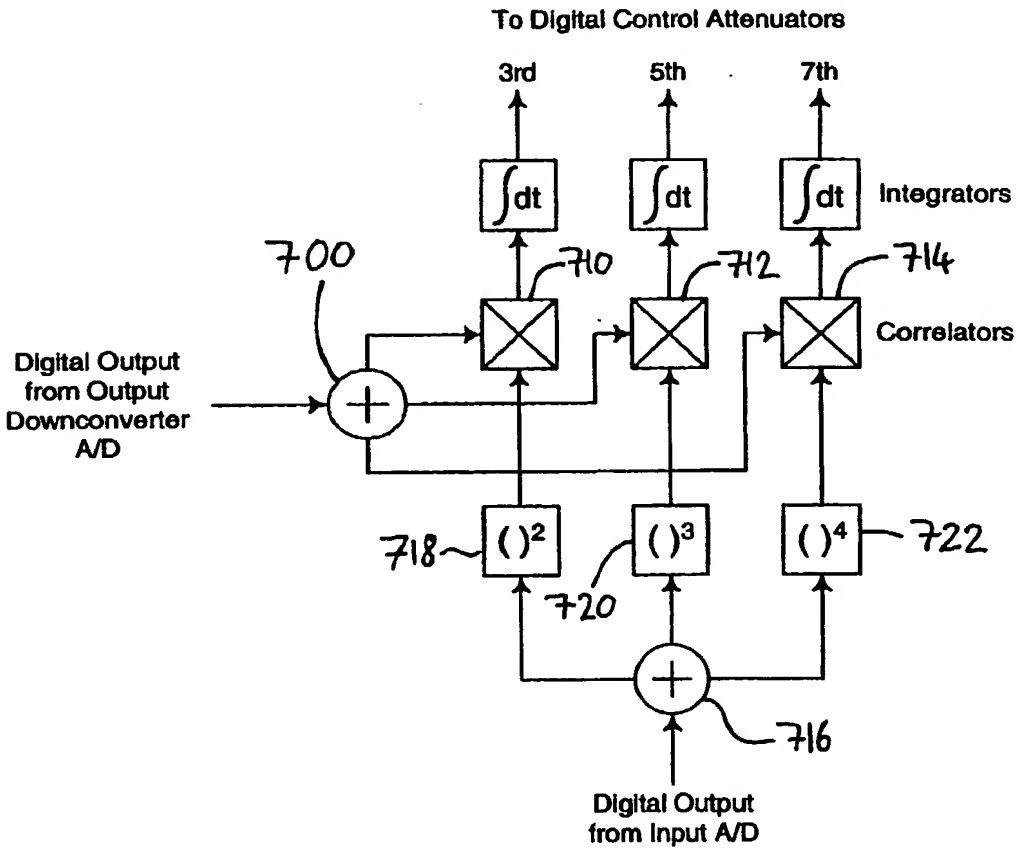

To Digital Control Attenuators
3rd
5th
7th
∫dt
∫dt
∫dt
Integrators
700
710
712
714
Correlators
Digital Output
from Output
Downconverter
A/D
718
()²
()³
()⁴
722
720
716
Digital Output
from Input A/D

Figure 7

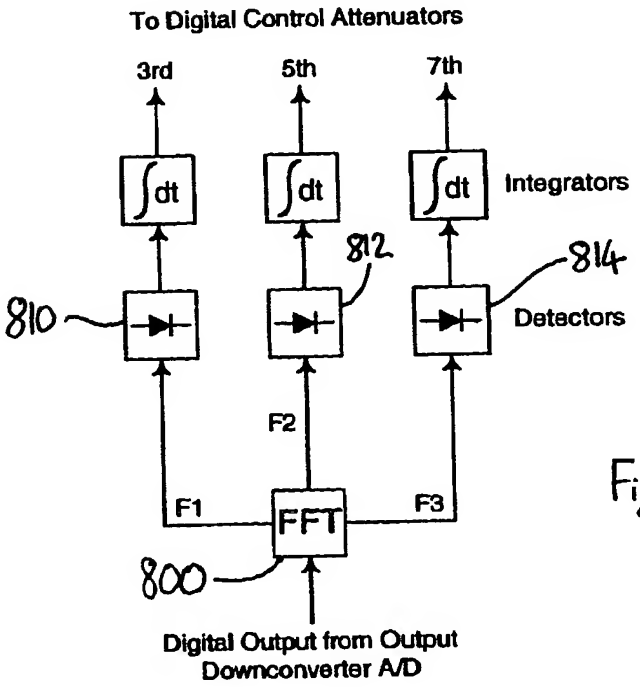


Figure 8

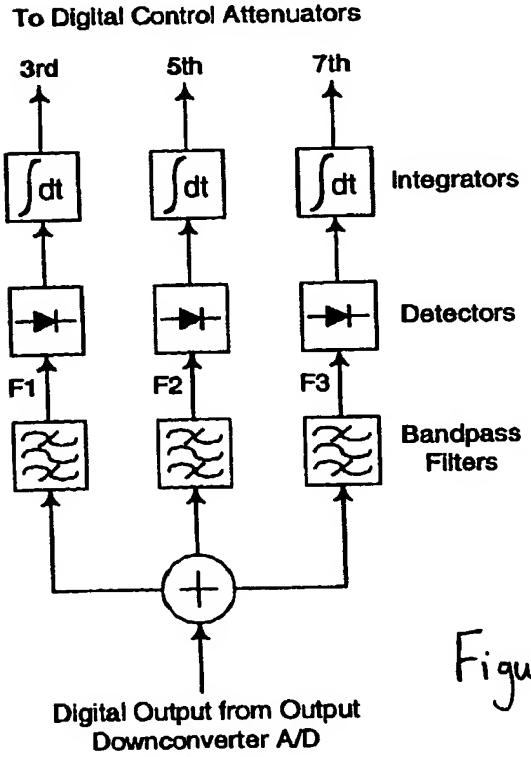


Figure 9

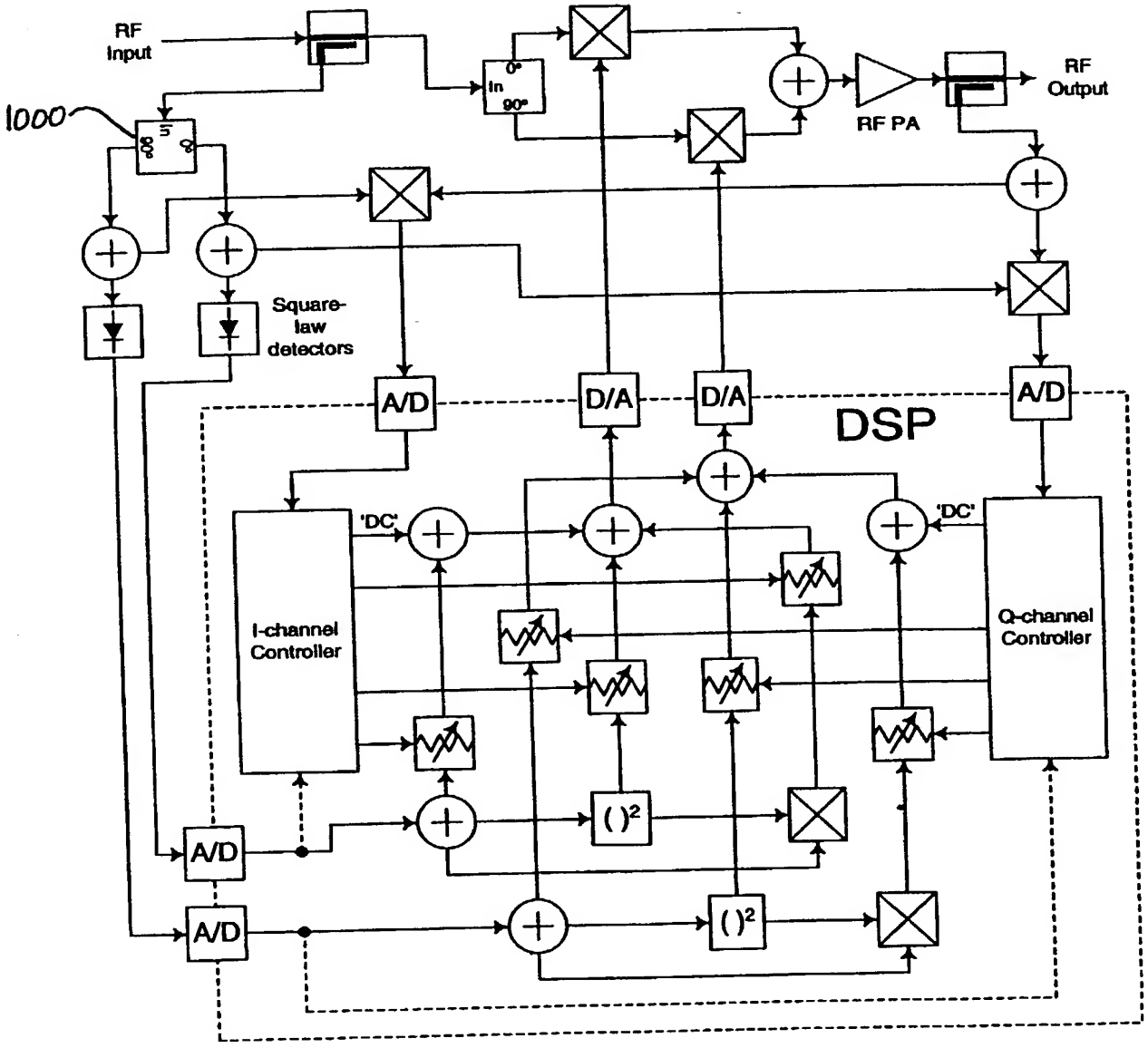
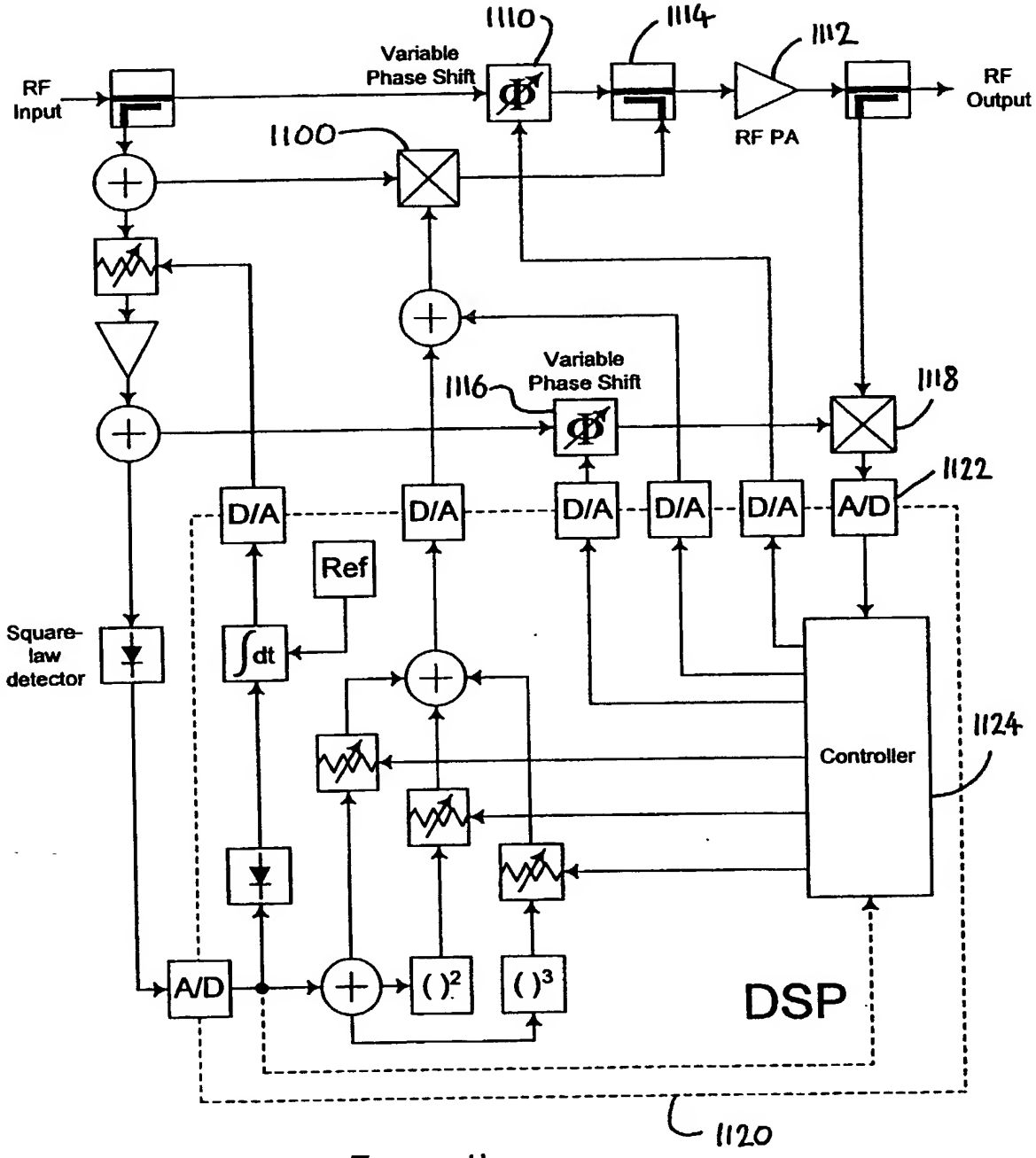

RF Input
1000
0°
In
90°
RF PA
RF Output
Square-law detectors
A/D
D/A
D/A
A/D
DSP
'DC'
'DC'
I-channel Controller
Q-channel Controller
A/D
A/D
()²
()²

Figure 10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1114
1112
Variable Phase Shift
RF Input
RF Output
RF PA
1100
Variable Phase Shift
1116
1118
1122
D/A
D/A
D/A
D/A
D/A
A/D
Ref
Square-law detector
∫dt
Controller
1124
A/D
( )²
( )³
DSP
1120

Figure 11

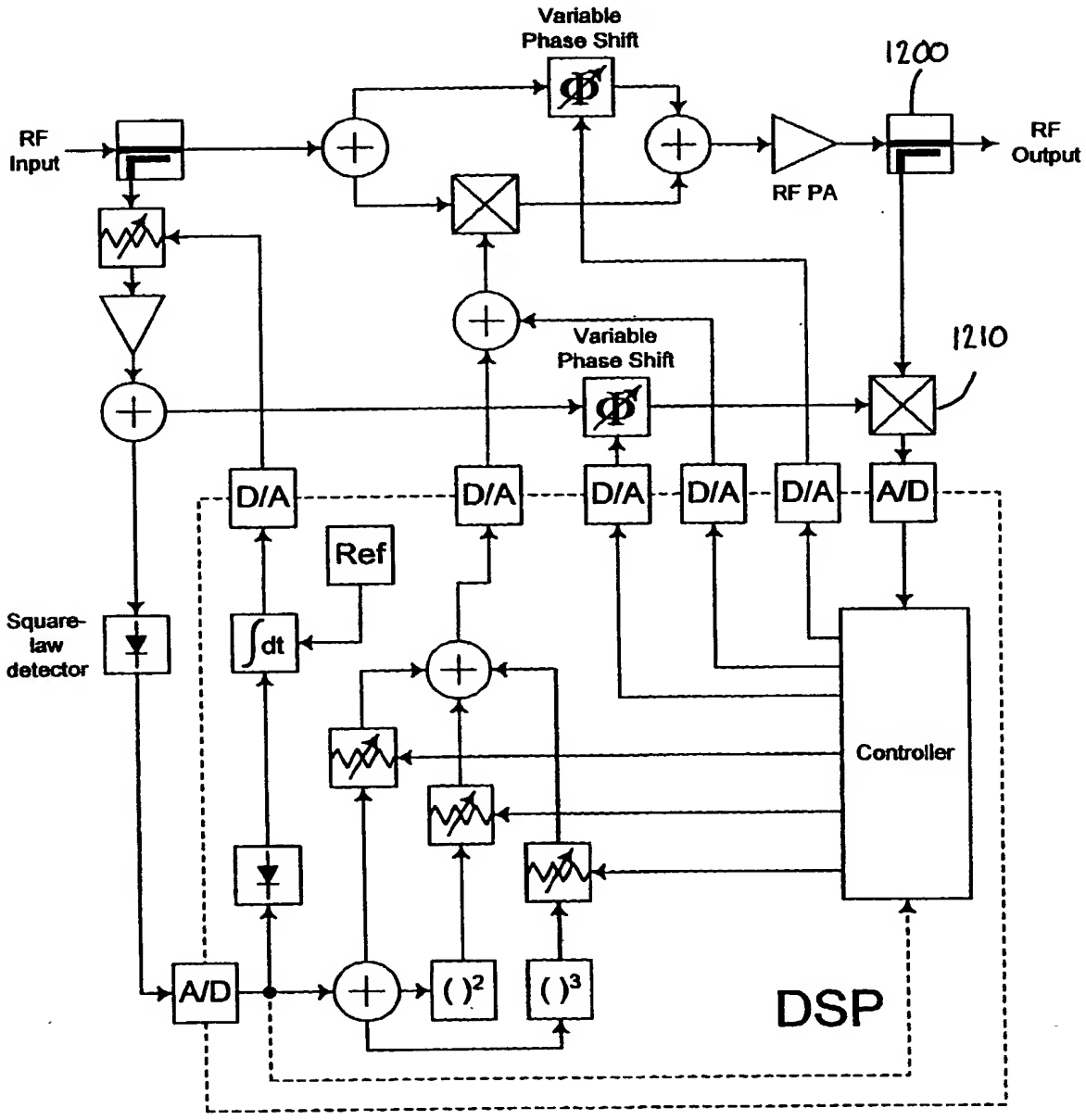
Variable
Phase Shift
1200
RF
Input
RF
Output
RF PA
Variable
Phase Shift
1210
D/A
D/A
D/A
D/A
D/A
A/D
Ref
Square-
law
detector
∫dt
Controller
A/D
( )²
( )³
DSP

Figure 12

DECLARATION AND POWER OF ATTORNEY

Attorney's Docket No. ~~23890~~ 46309/271492

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name. I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **A LINEARISER FOR A SIGNAL HANDLING APPARATUS**, the specification of which

☐ is attached hereto.

☒ was filed on 3/13/2002 as national phase of PCT International Application No. PCT/GB00/03528 and assigned Application No. 10/088,424 and was amended (if applicable) on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I do not know and do not believe that the same was ever known or used by others in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to the date of this application. I further state that the invention was not in public use or on sale in the United States of America more than one year prior to the date of this application. *I understand that I have a duty of candor and good faith toward the Patent and Trademark Office,* and I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code §119(a)-(d) or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor's certificate disclosing subject matter in common with the above-identified specification and having a filing date before that of the application on which priority is claimed:

Country	App. No.	Date of Filing	Priority Claimed Under 35 USC §119
Great Britain	9921570.9	13/09/99	Yes X No

I hereby claim the benefit under Title 35, United States Code, § 120 of any prior United States application(s), or §365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each claim of the present application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations §1.56, which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Application No.	Filing Date	Status: patented, pending, abandoned

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statement were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patents issuing thereon.

I hereby authorize the U.S. attorneys named herein to accept and follow instructions from **Withers & Rogers**, as to any action to be taken in the Patent and Trademark Office regarding this application, without direct communication between the U.S. attorney and the undersigned. In the event of a change in the persons from whom instructions may be taken, the U.S. attorney named herein will be notified by the undersigned.

POWER OF ATTORNEY: The following attorneys are hereby appointed to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: **Customer Number 23370**

Direct all correspondence to: **Customer Number 23370**

AFFIX BAR CODE LABEL HERE

23370
PATENT TRADEMARK OFFICE

Direct telephone calls at **404-815-6500**, to **Roger T. Frost**

Full name of sole or first inventor: Peter KENINGTON	
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☒ Additional inventors are being named on separately numbered sheets attached hereto.

2.00

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3.00

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